

Code: EC5T1

**III B.Tech - I Semester – Regular/Supplementary Examinations
October 2018**

**LINEAR INTEGRATED CIRCUITS
(ELECTRONICS & COMMUNICATION ENGINEERING)**

Duration: 3 hours

Max. Marks: 70

PART – A

Answer *all* the questions. All questions carry equal marks

11x 2 = 22 M

1.

- a) Define slew rate of Op-Amp.
- b) What is the need of level translator in Op-Amp?
- c) What is PSRR of Op-Amp.
- d) Draw the circuit of integrator with an Op-Amp.
- e) Why open-loop op-amp configuration is not used in linear applications?
- f) Draw the circuit diagram of a second order high pass filter.
- g) List the applications of All pass filters.
- h) Draw the pin diagram of 555 timer.
- i) What is the purpose of low pass filter in a phase locked loop?
- j) What are the specifications of IC AD 574(12 bit ADC)?
- k) Define Resolution and Linearity related to DAC.

PART – B

Answer any **THREE** questions. All questions carry equal marks.

$$3 \times 16 = 48 \text{ M}$$

2. a) Draw the ac equivalent circuit of dual input unbalanced output differential amplifier and derive the expressions for small signal voltage gain and input resistance. 10 M
- b) Explain the following in detail
- i) Input offset voltage
 - ii) Input offset current
 - iii) CMRR
- 6 M
3. a) Draw the circuit of Log and Anti log Amplifiers. Explain its operation. 8 M
- b) Explain the operation of Instrumentation amplifier with the help of block diagram and derive equation for gain. 8 M
4. a) Design a first order High pass filter with cutoff frequency of 1KHz and pass band gain of 11. Also draw its frequency response. 8 M
- b) Explain the principle of switched capacitor filters and list their advantages. 8 M
5. a) Explain the working of 555 timer as Astable multivibrator with neat diagram. 8 M

- b) What is frequency translation and explain FSK demodulation using 565 PLL. 8 M
6. a) Draw the circuit of weighted resistor DAC and derive expression for output-analog voltage. 8 M
- b) With a neat block diagram explain the data conversion procedure for dual slope ADC. 8 M